For purposes of example, and without limitation, certain example embodiments of this invention relate to a tape carrier package wherein a semiconductor chip is mounted on an insulating tape, where no hole is provided in the insulating tape under the semiconductor chip. Thus, when sealing resin is applied, the resin fills the gap between the bottom of the chip and the insulating tape. In the Fig. 1-2 embodiment of the instant application, for example, dummy pattern(s) 19 are provided adjacent corner(s) of the chip 14 in order to decrease the flow velocity of the resin 18, and thus reduce the number of air bubbles in the sealing resin of the final product in the area between the bottom of the chip and the insulating tape 11 (e.g., pg. 18, lines 5-17). In the Fig. 1-2 embodiment, the dummy pattern(s) 19 are entirely outside of the periphery of chip 14, so that the entire top surface of each dummy pattern 19 is covered by the sealing resin 18 in the final product. Locating the dummy pattern(s) in approximately such a position is helpful in reducing resin flow velocity, and thus reducing air bubbles in the final cured resin. In the Fig. 6-8 embodiments, the dummy pattern(s) 22 is partially inside and partially outside the periphery of the chip 14. In the Fig. 9 embodiment, the resin flow restricting pattern(s) 47 is/are made up of projections extending from inner leads 45. In the Fig. 10 embodiment, no dummy patterns are present, but the inner edge 53 of the solder resist is shaped in a zig-zag manner adjacent the corner of the chip in order to reduce resin flow velocity and thereby reduce air bubbles in the final cured resin. In the Fig. 12-14 embodiments, dummy patterns 67 separate from the inner leads, and projections 68, 70, 72 extending from the inner leads are used in combination to reduce resin flow velocity and thus air bubbles in the final cured resin.

Claim 9

Claim 9 stands rejected under 35 U.S.C. Section 103(a) as being allegedly unpatentable over Sozansky. This Section 103(a) rejection is respectfully traversed for at least the following reasons.

Claim 9 requires that "a first edge of said opening in the solder resist adjacent a corner of the semiconductor element is located nearer to the corner than a second edge of said opening in the solder resist adjacent the corner different than the first edge so as to control flow of resin from the corner to a space between a surface of the semiconductor element and the insulating tape during resin sealing." For example, see Fig. 10 of the instant application which illustrates than a first edge of the opening (see the zig-zag opening in solder resist 53 adjacent each corner) if closer to the corner of semiconductor element 52 than a different second edge of the opening (see also pg. 22, lines 13-15).

Sozansky fails to disclose or suggest this aspect of claim 9. In Sozansky, both edges of solder mask 22 adjacent a corner are the same distance from the corner, which is the opposite of what claim 9 calls for.

Claim 10

Claim 10 stands rejected under 35 U.S.C. Section 103(a) as being allegedly unpatentable over Sozansky in view of Hayakawa. The Office Action contends that it would have been obvious to have used Hayakawa's projections 22 which extend from leads 10 in order to restrict resin flow in Sozansky. This Section 103(a) rejection is respectfully traversed for at least the following reasons.

Sozansky relates to a device where the PCB 10 under the chip 12 does not have an aperture defined therein. Thus, in Sozansky (like the invention of claim 10), resin flows into and cures in the gap between the chip 12 and the PCB 10. In contrast, Hayakawa relates to a device where an aperture is defined in the tape 12 below chip 14. Thus, the purpose of Hayakawa's resin flow blocking members 20, 22 is to inhibit the resin from flowing into the area under the chip 14 since there is no tape under the chip. Since Sozansky wants resin to flow beneath the chip, one of ordinary skill in the art would never have used Hayakawa's restricting members (whose purpose is to prevent resin from flowing under the chip) in the device of Sozansky. Because one of ordinary skill in the art would never have used Hayakawa's restricting members in Sozansky for this reason, the Section 103(a) combination of Sozansky and Hayakawa is fundamentally flawed. Moreover, neither of these references discloses limiting resin flow in order to reduce air bubbles in the final cured resin in an area under the chip as in claim 10. The Section 103(a) rejection is fundamentally flawed for this reason as well. cordingly, the client may wish to consider traversing the Section 103(a) combination of Sozansky and Hayakawa for the reasons discussed above. The client may also wish to consider amending claim 10 to state that there is no aperture in the tape under the chip, so that resin fills the gap between the bottom of the chip and the tape, and so that the wider section(s) of the inner lead(s) reduce air bubbles in the resin located in this gap. The amendment to claim 10 would appear to further define over the cited art (especially Hayakawa), and emphasize the problems with the combination of these two references.

Claim 1

Claim 1 stands rejected under 35 U.S.C. Section 103(a) as being allegedly unpatentable over Sozansky in view of Sato. This Section 103(a) rejection is respectfully traversed for at least the following reasons.

There is no motivation or suggestion present in the art of record which would have led one of ordinary skill in the art to combine Sozansky and Sato as alleged in the Office Action to meet the invention of claim 1. The dummy bond pads 28 of Sozansky are provided to control the chip/board standoff height (col. 6, lines 42-47). In contrast, the protective dummy member 2 of Sato is a protrusion provided for protecting the ball grid array during fabrication of the package (e.g., col. 1, lines 38-40). On the other hand, the dummy pattern(s) of claim 1 is/are for *controlling (e.g., decreasing) the resin flow velocity*. Thus, the dummy patterns of the cited references function in an entirely different way than the dummy pattern(s) of claim 1. Thus, even if the references were combined as alleged in the Office Action, the invention of claim 1 still would not be met. Moreover, there is not suggestion present in the art of record for combining these references as alleged in the Office Action.

Claim 21

New claim 21 requires "a dummy pattern supported by the insulating tape adjacent a corner of the semiconductor element so as to control flow of the resin from the corner to a space between a surface of the semiconductor element and the insulating tape during resin sealing, and wherein at least part of the dummy pattern is located laterally beyond a periphery of the semiconductor element so that at least part of an upper surface of the

dummy pattern is covered with the resin." For example, in Fig. 2 of the instant application, at least part of dummy pattern 19 is located laterally beyond the periphery of the semiconductor element 14 so that at least part of the upper surface of the dummy pattern 19 is covered with resin 18.

Both Sozansky and Sato fail to disclose or suggest this aspect of claim 21. Thus, even if the references were combined as alleged in the Office Action, the invention of claim 21 still would not be met. With respect to Hayakawa, this reference does disclose blocking member 20. However, Hayakawa significantly differ from certain embodiments of this invention in that Hayakawa's structure includes an aperture in the tape under the chip. Thus, Hayakawa restricts resin flow in order to prevent the resin from making its way under the chip – which is the opposite of the invention of claim 21 which intends for the resin to flow and cure in an area under the entire chip.

For at least the foregoing reasons, it is respectfully requested that all rejections be withdrawn. All claims are in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

**NIXON & VANDERHYE P.C.**

By: _____
Joseph A. Rhoa
Reg. No. 37,515

JAR:caj
1100 North Glebe Road, 8th Floor
Arlington, VA 22201-4714
Telephone: (703) 816-4000
Facsimile: (703) 816-4100

## VERSION WITH MARKINGS TO SHOW CHANGES MADE

## IN THE CLAIMS

1. (Amended) A tape, for chip on film, on which a semiconductor element is mounted and resin is applied for sealing the semiconductor element, the tape for chip on film comprising:

an insulating tape, wherein the semiconductor element is supported by the insulating tape and no aperture is defined in the insulating tape in an area under the semiconductor element;

a plurality of wiring patterns formed on the insulating tape;

a solder resist partially covering the wiring patterns [by application to have] in a form such that an opening is defined in the solder resist at least in all or part of an area under the semiconductor element; and

a dummy pattern [provided at] supported by the insulating tape adjacent a corner of a region for the semiconductor element to be mounted so as to control flow of the resin from the corner to a space between a surface of the semiconductor element and the insulating tape during resin sealing.

2. (Amended) The tape for chip on film as defined in claim 1, wherein the dummy pattern is provided independent of the wiring patterns and the solder resist so that the dummy pattern is not in electrical communication with the wiring patterns or the solder resist.

9. (Amended) A tape for chip on film on which a semiconductor element is mounted and resin is applied for sealing the semiconductor element, the tape for chip on film comprising:

an insulating tape;

a plurality of wiring patterns formed on the insulating tape; and

a solder resist partially covering the wiring patterns, wherein [by application to have] an opening is defined in the solder resist in an area under the semiconductor element, wherein

a first[an opening] edge of said opening in the solder resist [opposed to] adjacent a corner of [a region for] the semiconductor element [to be mounted is located in a vicinity of the corner, and a]is located nearer to the corner than a second edge of said opening in the solder resist adjacent the corner different than the first edge [shape of the opening edge of the solder resist in the vicinity of the corner is made along a shape of the corner ]so as to control flow of resin from the corner to a space between a surface of the semiconductor element and the insulating tape during resin sealing.

10. (Amended) A tape for chip on film on which a semiconductor element is mounted and resin is applied for sealing the semiconductor element, the tape for chip on film comprising:

an insulating tape, wherein the semiconductor element is supported by the insulating tape and no aperture is defined in the insulating tape in an area under the semiconductor element;

a plurality of wiring patterns formed on the insulating tape;

a solder resist partially covering the wiring patterns, wherein [by application to have] an opening is defined in the solder resist at least in all or part of an area under the semiconductor element; and

an inner lead in a wiring pattern located on a specified side of [a region for] the semiconductor element [to be mounted] is at least partially located inside the opening [of]defined in the solder resist, wherein

the inner lead has a large width section wider than an electric connection section of the inner lead connected to the semiconductor element so as to control flow of resin from the specified side to a space between a surface of the semiconductor element and the insulating tape during resin sealing, so that air bubbles in the resin located in a gap between a surface of the semiconductor element and the insulating tape can be reduced.

11. (Amended) The tape for chip on film as defined in claim 10, wherein the large width section of the inner lead is disposed either outside or inside a border line of [the]a region for the semiconductor element to be mounted, or from outside to inside the border line of the region.

Please add the following new claims:

19. (New) The tape for chip on film of claim 1, wherein the entire dummy pattern is located laterally beyond the periphery of the semiconductor element.

20. (New) The tape for chip on film of claim 1, wherein the dummy pattern is not part of, and is not connected to, the semiconductor element.

21. (New) A tape, for chip on film, on which a semiconductor element is mounted and resin is applied for sealing the semiconductor element, the tape for chip on film comprising:

an insulating tape, wherein the semiconductor element is supported by the insulating tape and no aperture is defined in the insulating tape in an area under the semiconductor element;

a plurality of wiring patterns formed on the insulating tape;

a solder resist partially covering the wiring patterns in a form such that an opening is defined in the solder resist at least in all or part of an area under the semiconductor element; and

a dummy pattern supported by the insulating tape adjacent a corner of the semiconductor element so as to control flow of the resin from the corner to a space between a surface of the semiconductor element and the insulating tape during resin sealing, and wherein at least part of the dummy pattern is located laterally beyond a

periphery of the semiconductor element so that at least part of an upper surface of the dummy pattern is covered with the resin.

22. (New) The tape for chip on film of claim 6, wherein the wiring pattern, the inner lead, and the dummy pattern are fixed to the insulating tape without use of an adhesive.

23. (New) The tape for chip on film of claim 6, wherein the wiring pattern, the inner lead, and the dummy pattern are fixed to the insulating tape with use of an adhesive.

24. (New) The tape for chip on film of claim 8, wherein the wiring pattern, the inner lead, and the dummy pattern are fixed to the insulating tape without use of an adhesive.

25. (New) The tape for chip on film of claim 8, wherein the wiring pattern, the inner lead, and the dummy pattern are fixed to the insulating tape with use of an adhesive.

26. (New) A semiconductor device comprising a semiconductor element mounted on the tape for chip on film as defined in claim 9 and sealed with resin.

27. (New) A semiconductor device comprising a semiconductor element mounted on the tape for chip on film as defined in claim 10 and sealed with resin.

28. (New) The tape for chip on film of claim 10, wherein the entire dummy pattern is located laterally beyond the periphery of the semiconductor element.

29. (New) The tape for chip on film of claim 11, wherein the entire dummy pattern is located under the semiconductor element without contacting the semiconductor element.